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10/693,022	10/23/2003	Vladimir Bulovic	Y2086-10301	1746

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EXAMINER	
BODDIE, WILLIAM	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,022	BULOVIC ET AL.	
	Examiner	Art Unit	
	William Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/23/03, 8/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 7-11, 13-17, 19-20, 22-24 and 26-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Tamura et al. (US 2002/0130326).

With respect to claim 1, Tamura discloses, an array, comprising:

a plurality of light emitting devices (12-14 in fig. 3a,b) disposed over a substrate (10 in fig. 3b); and

a photodetector (15-17 in fig. 3a/b) that detects light emitted through the substrate from the light emitting devices (para. 45).

With respect to claim 2, Tamura discloses, the array of claim 1 (see above), wherein the substrate has an upper surface (10 in fig. 3b), and the plurality of light emitting devices (12-14 in fig. 3b) are formed over the upper surface of the substrate (clear from fig. 3b).

With respect to claim 3, Tamura discloses, the array of claim 2 (see above), wherein the substrate has a side surface (cross-hatching 10 in fig. 3b) formed substantially perpendicular to the upper surface (clear from fig. 3b), and the photodetector (16 in fig. 3b) is formed on the side surface of the substrate.

With respect to claim 4, Tamura discloses, the array of claim 2 (see above), wherein the photodetector (9 in fig. 2a/b) is formed over the upper surface of the substrate (10 in fig. 2b).

With respect to claim 5, Tamura discloses, the array of claim 1 (see above), wherein the photodetector includes a plurality of photodetectors (15, 16 and 17 in fig. 3a; para. 53).

With respect to claim 7, Tamura discloses, the array of claim 5 (see above), wherein the substrate (10 in fig. 2a/b) has an upper surface, and the plurality of photodetectors (9 in fig. 2a) are formed over outer periphery edges (clear from fig. 2a/b) of the upper surface (col. 6, lines 7-16).

With respect to claim 8, Tamura discloses, the array of claim 1 (see above), further comprising a feedback circuit (5 in fig. 1) that measures a brightness level for each of the plurality of light emitting devices and varies a voltage applied to individual ones of the light emitting devise to maintain a brightness level of each of the light emitting devices at a substantially constant level (paras. 12-13).

With respect to claim 9, Tamura discloses, the array of claim 8 (see above), wherein the substrate has an upper surface (10 in fig. 2a/b), and the plurality of light emitting devices (8 in fig. 2a/b) are formed over the upper surface of the substrate (clear from fig. 2b).

With respect to claim 10, Tamura discloses, the array of claim 8 (see above), wherein the substrate has an upper surface (10 in fig. 3b), and the photodetector (16 in fig. 3b) is formed on the side surface of the substrate (clear from figs. 3a/b).

With respect to claim 11, Tamura discloses, the array of claim 8 (see above), wherein the photodetector (9 in fig. 2b) is formed on the upper surface of the substrate (7 in fig. 2b).

With respect to claim 13, Tamura discloses, a display (col. 1, lines 6-8) comprising the array of claim 1 (see above).

With respect to claim 14, Tamura discloses, a method for forming an array, comprising:

forming a plurality of light emitting devices (8 in fig. 2a/b) disposed over a substrate (10 in fig. 2b); and

forming a photodetector (9 in fig. 2a/b) that detects light emitted through the substrate from the light emitting devices (para. 45).

With respect to claims 15-17 and 19-20, these claims are seen as recitations of claims 2, 3, 5 and 7-8 respectively. As such claims 15-17 and 19-20 are rejected on the same merits shown above in their sister claims.

With respect to claim 22, Tamura discloses, a method for maintaining a substantially constant brightness in a plurality of light emitting devices (8 in fig. 2a/b) disposed over the upper surface of a substrate (10 in fig. 2b) in an array, comprising:

measuring light emitted through the substrate from each of the light emitting devices (9 in fig. 2a/b; para. 12); and

varying the voltage level applied to each of the light emitting devices to maintain a substantially constant brightness level of light emitted from the light emitting devices (col. 2, lines 26-28; para. 40).

With respect to claims 23-24 and 26, these claims are seen as recitations of claims 3, 11 and 7 respectively. As such claims 23-24 and 26 are rejected on the same merits shown above in their sister claims.

With respect to claim 27, Tamura discloses, the method of claim 22 (see above), wherein varying the voltage level applied to each of the light emitting devices comprises generating a compensation factor for each of the light emitting devices (para. 40) and applying the compensation factor to a voltage applied to the corresponding light emitting device (para. 40).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6, 18, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US 2002/0130326) in view of Cok (US 7,026,597).

With respect to claim 6, Tamura discloses, the array of claim 5 (see above), wherein the substrate has an upper surface and a plurality of side surfaces (cross-hatching 10 in fig. 3b), each of the side surfaces being substantially perpendicular to the upper surface (clear from fig. 3b), and at least one of the photodetectors is formed on a the side surface (16 in fig. 3b).

Tamura does not expressly disclose, that the photo detectors are formed on each side surface.

Cok discloses, forming photodetectors on each edge of a display (20 in fig. 5).

Cok and Tamura are analogous art because they are from the same field of endeavor namely, placement of photodetectors within a display.

At the time of the invention it would have been obvious to one of ordinary skill in the art to place Tamura's photodetectors along each side of the display as disclosed by Cok.

The motivation for doing so would have been improved illumination detection (Cok; col. 1, lines 65-67).

Therefore it would have been obvious to combine Cok with Tamura for the benefit of improved illumination detection to obtain the invention as specified in claim 6.

With respect to claim 18, as shown above Tamura discloses claim 17. The further limitations of claim 18 are identical to those of claim 6. Therefore claim 18 is rejected on the same merits shown above in claim 6.

With respect to claim 25, as shown above Tamura discloses claim 22. The further limitations of claim 25 are identical to those of claim 6. Therefore claim 25 is rejected on the same merits shown above in claim 6.

5. Claims 12 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US 2002/0130326) in view of Yamazaki et al. (US 6,424,326).

With respect to claim 12, Tamura discloses, the array of claim 8 (see above), wherein the feedback circuit (5 in fig. 1) includes a compensation factor generator (5 in fig. 1) for generating a compensation factor for each of the of the plurality of light emitting devices (para. 40).

Tamura does not expressly disclose, a memory array for storing the compensation factor for each of the plurality of light emitting devices.

Yamazaki discloses, a display detecting brightness (fig. 1) and a memory array (204 in fig. 6) for storing a compensation factor for each of the plurality of light emitting devices (col. 12, lines 21-55).

Yamazaki and Tamura are analogous art because they are both directed to a similar problem solving area, namely correcting uneven display luminance.

At the time of the invention it would have been obvious to one of ordinary skill in the art to store the correction factors generated by Tamura in a memory array as taught by Yamazaki.

The motivation for doing so would have been to store an ideal luminance to compare the current state of the display against, thus achieving a more uniform and ideal luminance (Yamazaki; col. 12, lines 28-44).

At the time of the invention it would have been obvious to combine Yamazaki with Tamura for the benefit of a more uniform and ideal luminance to obtain the invention as specified in claim 12.

With respect to claim 21, as shown above Tamura discloses claim 14. The further limitations of claim 21 are identical to those of claim 12. Therefore claim 21 is rejected on the same merits shown above in claim 12.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yuyama (US 6,069,676) discloses a colored display with photo detectors at various locations.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wlb
4/17/06

AMR A. AWAD
PRIMARY EXAMINER